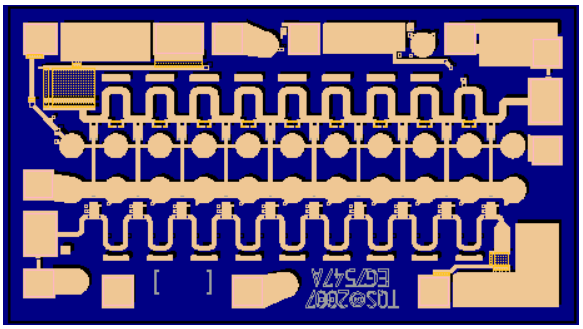
TGA4842

DC - 35 GHz Wideband Amplifier



Product Description

The TriQuint TGA4842 is a medium power wideband AGC MMIC. Drain bias may be applied through the output port for best efficiency or through the on-chip drain termination. RF ports are DC coupled enabling the user to customize system corner frequencies. The TGA4842 requires off-chip decoupling and blocking components.

The TGA4842 is an excellent choice for 40Gb/s and 100Gb/s applications. The TGA4842 is capable of driving a modulator with an adjustable output voltage of 3-10 Vpp.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in die form.

Lead Free & RoHS Compliant.

Key Features and Performance

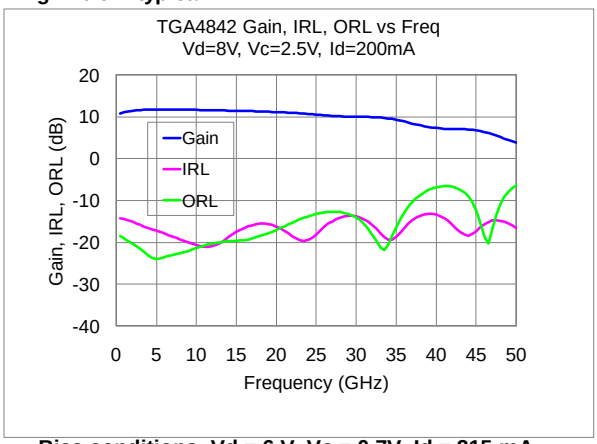
- 40 & 100Gb/s Optical Modulator Driver
- 0.15um Power pHEMT Technology
- Bias: Vd = 6 V, Id = 170 mA
- Chip Size: 1.80 x 1.00 x 0.1 mm

Primary Applications

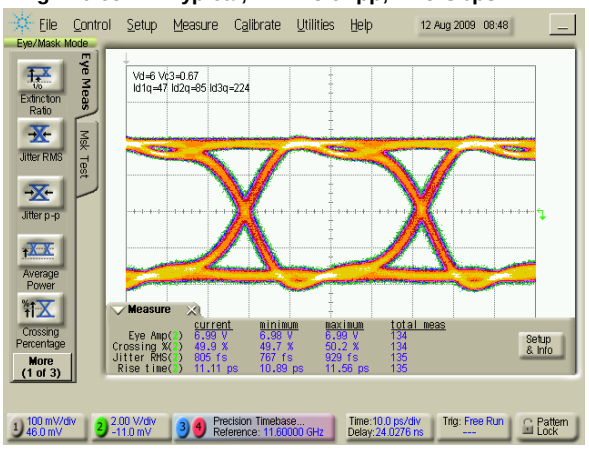
- 40Gb/s DPSK / DQPSK Driver
- 100Gb/s DP-QPSK Driver
- 40Gb/s Predriver or Gain Block
- Test Equipment

Measured Performance

Bias conditions: Vd = 8 V, Vc = 2.5 V, Id = 200 mA, Vg = -0.9 V typical



Bias conditions: Vd = 6 V, Vc = 0.7V, Id = 215 mA, Vg = -0.65 Vm Typical, Vin = 3.6Vpp, 21.5 Gbps



Datasheet subject to change without notice

Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd	Drain Voltage	9 V	2/ 3/ 4/
Vd-Vg	Drain to Gate Voltage	13 V	2/ 3/ 4/
Vg	Gate Voltage Range	-5 to 0 V	
Vc	Control Voltage Range	(Vd-7) to +5.5 V	3/ 4/
Id	Drain Current – Biased through on-chip drain termination (i.e. Using V+) Biased through Rfout using Bias Tee	 135 mA 270 mA	2/
Ig	Gate Current Range	-30 to 21 mA	
Ic	Control Current Range	-15 to 21 mA	
Vin_pp	Peak-Peak Input Voltage	7 V	
Pin	Input Continuous Wave Power	24 dBm	2/
Pd	Max Power Dissipation – Biased through on-chip drain termination (i.e. Using V+) Biased through Rfout using Bias Tee	 1.22 W 3.0 W	 5/ 6/
Tch	Maximum Channel Temperature	200 °C	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

3/ If Biasing through on-chip Drain Termination (i.e. using V+): Assure Vd – (Vc-0.34*Vg) – Id*50 $\leq$ 6.5 V,
If biasing through Rfout using Bias Tee: Assure Vd – (Vc-0.34*Vg) $\leq$ 6.5 V,

4/ Assure Vd-Vc >= -0.5.

5/ Maximum Power Dissipation if biased through V+ is based Max Vd * Max Id

6/ Maximum Power Dissipation if biased through Bias Tee is based upon Baseplate temperature of 70 °C and Channel Temperature of 200 °C, using the thermal resistance published in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value
Vd	Drain Voltage biased through RFout	6 V
Id	Drain Current	200 mA
Id_Drive	Drain Current under RF Drive	200 mA
Vc	Control Voltage	0.7 V
Vg	Gate Voltage	-0.8 V

Table III
RF Characterization Table

Bias: Vd = 8.5 V, Idq = 150 mA, Vc = 2.3 V, Vg = -1.8 V typical

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOMINAL	MAX	UNITS
Gain	Small Signal Gain	f = 0.1 - 20 GHz f = 20.1 - 30 GHz f = 30.1 - 35 GHz f = 35.1 - 40 GHz f = 40.1 – 50 GHz	8 8 7 4 -	11 10 9 6 4	- - - -	dB
IRL	Input Return Loss	f = 0.1 – 25 GHz f = 25.1 – 30 GHz f = 30.1 – 35 GHz f = 35.1 - 38 GHz f = 38.1 – 50 GHz	10 8 6 - -	15 15 15 10 6	- -	dB
ORL	Output Return Loss	f = 0.1 - 20 GHz f = 20.1 - 30 GHz f = 30.1 - 35 GHz f = 35.1 - 50 GHz	10 7 5 -	15 12 10 -	- -	dB
BW	3 dB Bandwidth	f(x) – f(1 GHz) = 3 dB x = freq of 3 dB BW	-	37	-	GHz

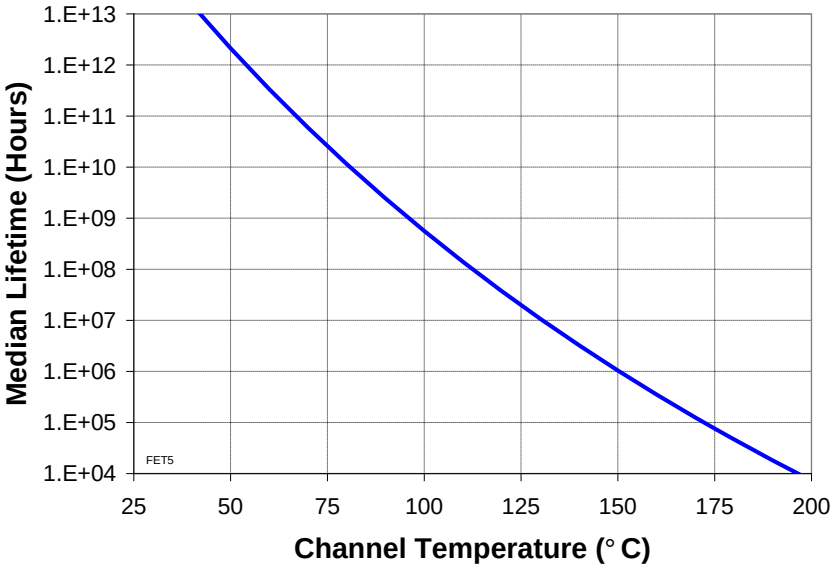
Table IV
Power Dissipation and Thermal Properties

Parameter	Test Conditions	Value	Notes
Thermal Resistance, θjc	Vd = 6 V Idq=170 mA Pd= 1.02 W Tbaseplate = 70 °C	θjc = 43.1 °C/W Tchannel = 114 °C Tm = 7.9 E+7 Hrs	1/, 2/
Thermal Resistance, θjc Under RF Drive	Vout = 7 Vpp, Vd = 6V Id = 170 mA Pd=0.9 W Tbaseplate = 70 °C	θjc = 43.1 °C/W Tchannel = 109 °C Tm = 1.6 E+8 Hrs	
Storage Temperature		-65 to 150 °C	

1/ Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

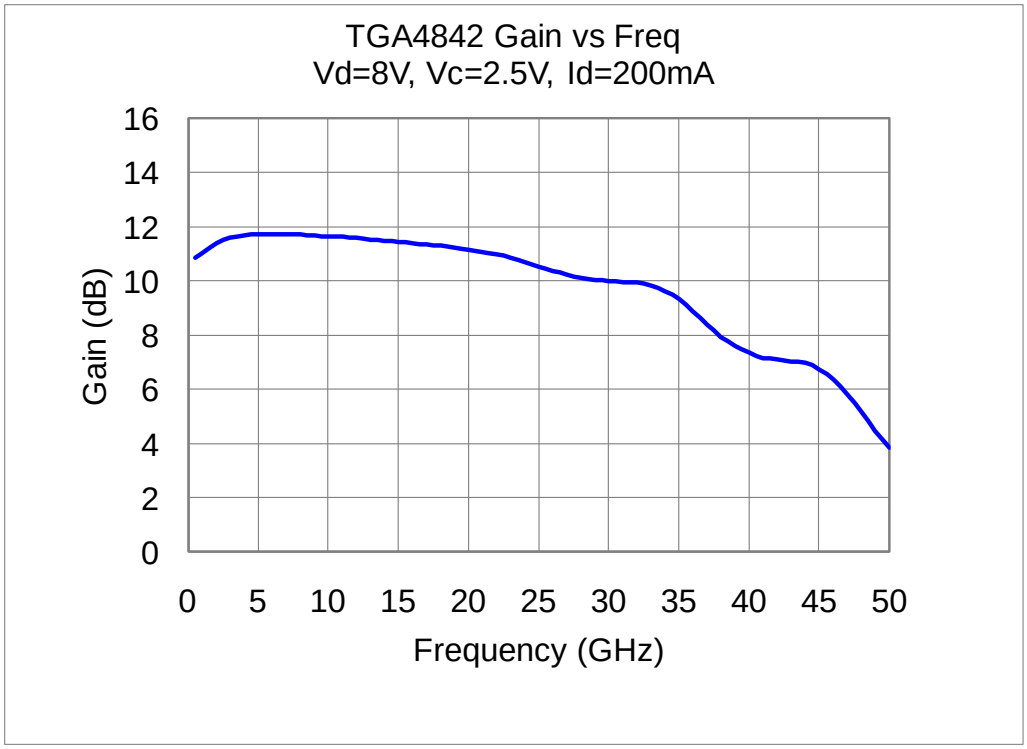
2/ θjc is the thermal resistance of the die mounted to a 0.020" thick Cu-Mo block using 0.8 mil conductive epoxy.
To calculate the temperature rise, calculate the dissipated power (Pdiss = Idq*Vd) and multiply by θjc. For example: Tbase = 70 °C, Idq = 170 mA, Vd = 6V. Pdiss= 1.02 W. θjc=43.1 °C/W. Temperature rise = θjc*Pdiss = 44 °C; Tchannel = Tbase + Temp rise = 114 °C

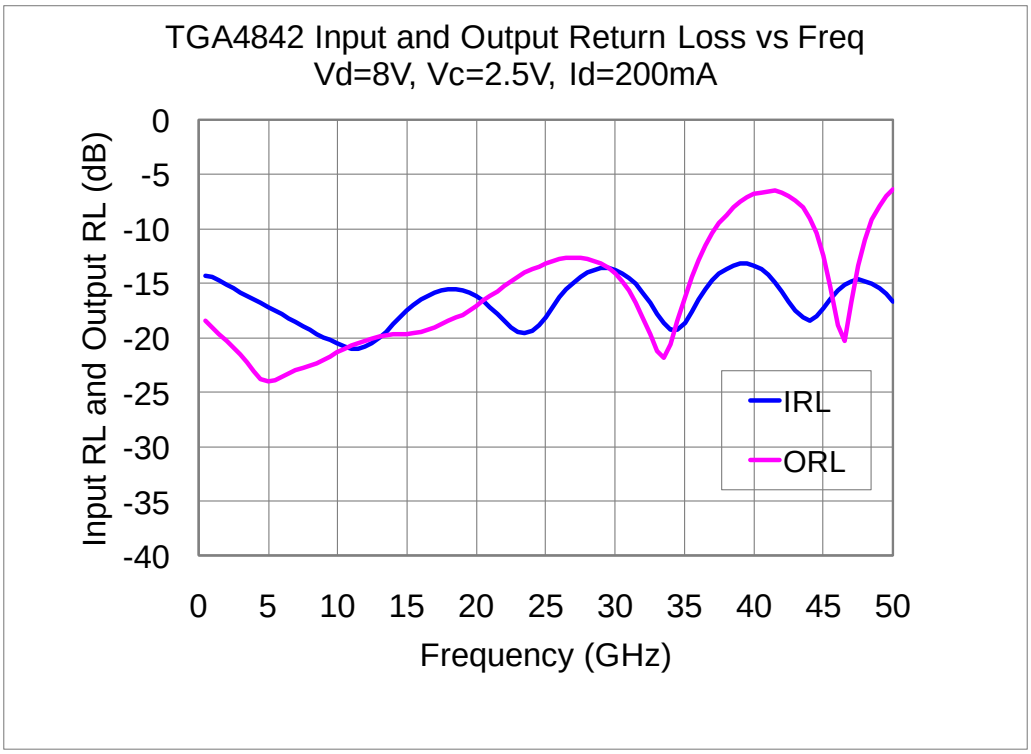
Median Lifetime (Tm) vs. Channel Temperature



Measured Performance

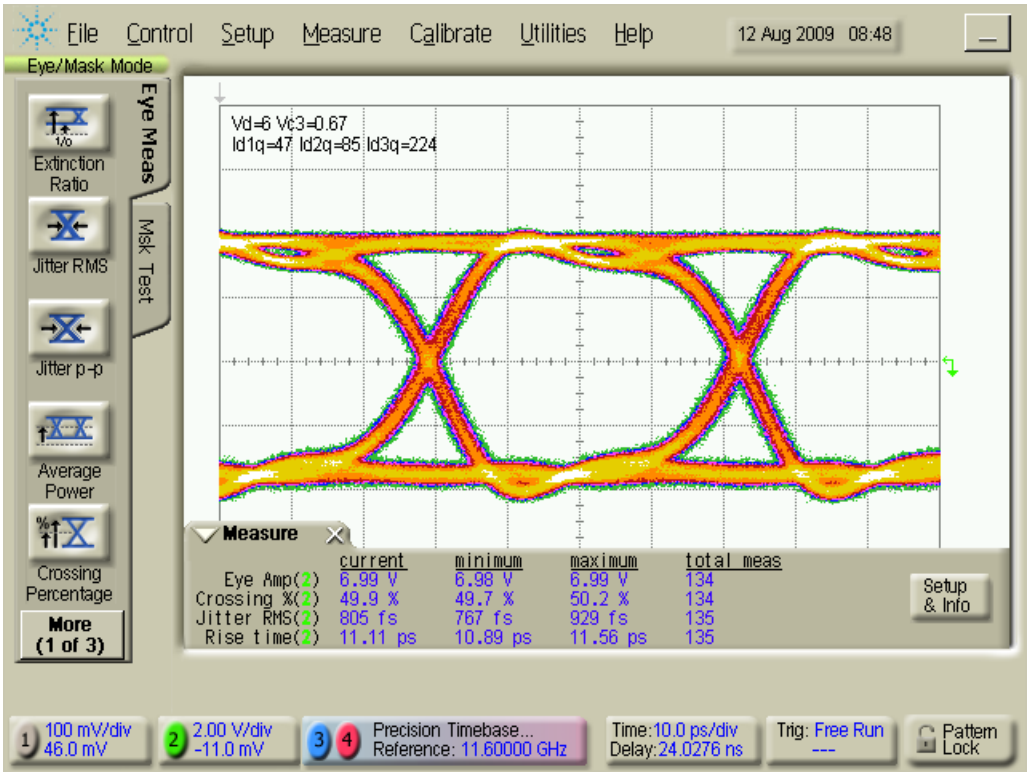
Bias conditions: Vd = 8 V, Vc = 2.5 V, Id = 200 mA, Vg = -0.9 V, Typical





Measured Performance

Bias conditions: Vd = 6 V, Vc = 0.7 V, Id = 220 mA, Vg = -0.65 V, Typical Vin = 3.6 Vpp, 21.5 Gbps



Recommended Bias Procedure

Bias ON

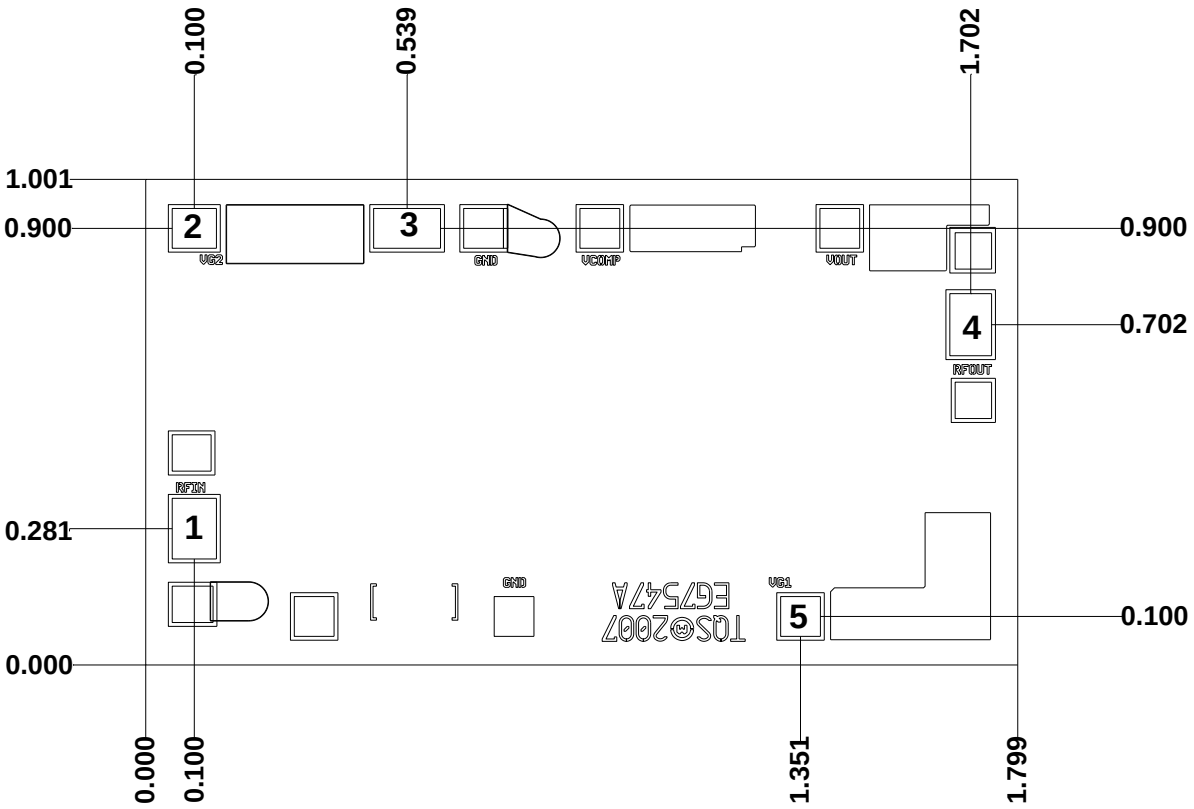
1. Disable the PPG
2. Set Vg=-3V
3. Apply Vd* either through Vd / RFout or through V+
4. Apply Vctrl
6. Make Vg more positive until Id reaches desired value.
7. Enable the PPG

Bias OFF

1. Disable the output of the PPG
2. Set Vctrl = 0V (if appliable)
3. Set Vd=0V
4. Set Vg=0V

*** Note:** Vd / RFout Bias operation requires a bias tee

Mechanical Drawing

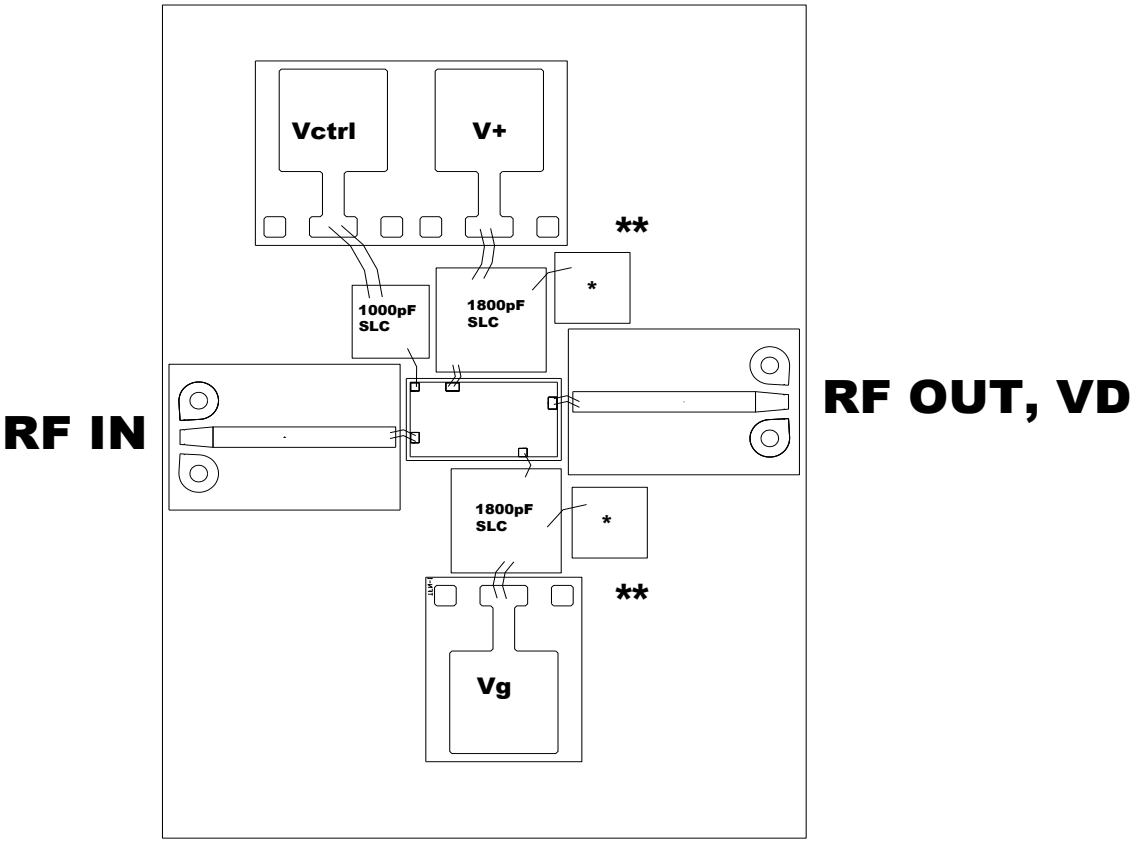


Units: millimeters
Chip edge to bond pad dimensions are shown to center of pad
Chip size tolerance: ± 0.051
Thickness: 0.100 (reference only)

GROUND IS BACKSIDE OF MMIC

Bond Pad #1:	Rfin	0.091 x 0.125
Bond Pad #2:	Vctrl	0.091 x 0.082
Bond Pad #3:	Vd_bypass	0.138 x 0.082
Bond Pad #4:	Rfout / Vd (Rfout)	0.086 x 0.128
Bond Pad #5:	Vg	0.082 x 0.082

Recommended Assembly Diagram



Note: Input and Output ports are DC coupled.

If biasing Vd through the Rfout side, a bias tee is required.

* Rec**ommend**ed Components:

* Capacitor value	Bypassing effective to:
None	20 MHz
0.01 uF	4 MHz
0.1 uF	250 KHz

** The part numbers of the off-chip caps are:

Part Number	Manufacturer
GZOSYC104KJ8182MAW	AVX
VB4080X7R105Z16VHX182	Presidio

Evaluation Platform Assembly Notes

Assembly Notes:

Reflow Attachment:

Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
Use alloy station or conveyor furnace with reducing atmosphere
No fluxes should be utilized
Coefficient of thermal expansion matching is critical for long-term reliability
Storage in dry nitrogen atmosphere

Adhesive Attachment:

Organic attachment can be used in low-power applications
Curing should be done in a convection oven; proper exhaust is a safety concern
Microwave or radiant curing should not be used because of differential heating
Coefficient of thermal expansion matching is critical

Component Pickup and Placement:

Vacuum pencil and/or vacuum collet preferred method of pick up
Avoidance of air bridges during placement
Force impact critical during auto placement

Interconnect:

Thermosonic ball bonding is the preferred interconnect technique
Force, time, and ultrasonics are critical parameters
Aluminum wire should not be used
Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
Maximum stage temperature: 200°C

Ordering Information

Part	ECCN
TGA4842	3A001.b.2.d